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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,488	04/12/2004	Haruo Togashi	09812.0405	3033

22852 7590 10/29/2007  
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER  
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901 NEW YORK AVENUE, NW  
WASHINGTON, DC 20001-4413

EXAMINER

PLANTE, JONATHAN R

ART UNIT	PAPER NUMBER
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2182

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10/29/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



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24

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EXAMINER
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ART UNIT	PAPER
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20071023

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**Commissioner for Patents**

The information disclosure statement filed 01 October 2007 to complies with 37 CFR 1.97(d) and 37 CFR 1.97(e).

It has been placed in the application file, and has been considered.

Upon review to the IDS in relation to the foreign references the Examiner notes, none of the references cited in the IDS teaches, in conjunction with all other claim elements the removing of a predetermined number of bit planes from the lower side and out putting the remaining bit planes in parallel allowing the quantity of generated codes per frame to be kept constant.

**KIM HUYNH  
SUPERVISORY PATENT EXAMINER**

10/23/07

/Jonathan R. Plante/  
Examiner Art Unit 2182